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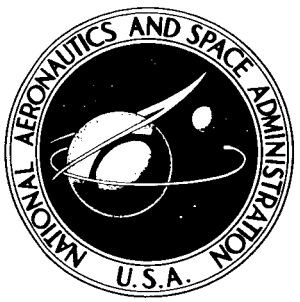

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LOW-POWER, LOW-LEVEL ANALOG-TO-DIGITAL CONVERTER FOR SPACE VEHICLE APPLICATIONS

by John C. Sturman and Anthony V. Bertolino

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SUMMARY

Design considerations and a detailed circuit description are presented for a seven-bit analog-to-digital converter with a 20-millivolt full-scale input. The special significance of this design is the achievement of a power level of less than 10 milliwatts for the complete converter when operating at a 250-word-per-second conversion rate. The prototype converter is built by using relatively conventional components in welded cordwood modules; however, the design could be readily adapted for thin film or possibly integrated circuit fabrication.

INTRODUCTION

The rapidly increasing data requirements of satellites and other space vehicles have been a major factor in the trend toward predominantly digital systems. Handling data in digital form has a number of advantages including increased potential accuracy of transmission, increased reliability, decreased power requirements, and the possibility of doing on-board computation or compression. To take full advantage of these features requires not only low-power logic elements for handling the digital data, but also a means of converting the analog voltage inputs into digital form while using a minimum of power. It was to fulfill this latter requirement that the analog-to-digital converter to be described was developed.

Although the primary purpose of this program was to investigate the lowest practical power limits for analog-to-digital conversion, some basic target goals were decided on to provide direction for the design. The converter was to be a complete unit capable of converting a 0 to 20 millivolt input into a seven-bit binary word 250 times per second. It was to be operable over the temperature range of -20° to $+80^{\circ}$ C with a total average power consumption of 50 milliwatts or less. No power supplies or other peripheral cir-

cuitry were to be provided as it was expected that the converter would be operated as part of a larger system in any given application. In addition, a primary power source at approximately 5 volts was postulated, and this value was used directly for the digital logic portions of the system.

The previous specifications were adopted partly because they represented a system that could have wide applicability to a number of space experiments and also because attainment of these goals would generate sufficient data on micropower systems for more specialized future applications.

Two other related factors were considered important in this design. They were the attainment of low heat generation and high reliability. Other investigators have built low-power converters (ref. 1), and a number of high-level (0 to 5 V) converters are available as standard items. No one else, to the authors' knowledge, has combined the features of both a low-level input and a low-power converter. Such a unit would have increased reliability because of the decreased thermal stress on the components, which is a prime argument in favor of micropower circuitry whether or not power consumption per se is a problem. Low power is also highly desirable for circuits that are to be microminiaturized and is one factor that makes the system to be described attractive for fabrication by integrated circuit techniques.

A second feature promoting reliability is the use of the minimum number of components consistent with system requirements and the attainment of micropower operation. This approach results in a number of different circuit blocks each designed to perform a specific function as compared to using a larger number of identical circuits to synthesize the desired logic functions. Although this philosophy of design is not presently favored for microcircuits, it is obviously correct for systems built with discrete components. Furthermore, it will probably prove best once integrated circuit fabrication techniques are improved to the point that many different circuits can be readily fabricated without sacrificing reliability.

Design of the logic form to be used in implementing this converter was predicated mainly on the requirement of extremely low-power operation. This led to the choice of a logic scheme that utilized predominantly digital elements, since circuits that are either fully on or fully off can be designed to dissipate very little power except when switching. On this basis the old but effective sequential approximation technique was selected as being the best choice for this application. The fact that the original goal was for a relatively slow-speed device was also in favor of this choice.

Converter operation is diagramed in figure 1. The converter compares the analog input voltage with an analog feedback voltage generated by a predominantly digital system. The clock and ring counter provide a sequence of pulses to program the operation of the converter. These pulses are gated into a storage register that controls a digital-to-analog conversion network, which approximates the input as 1 of 128 discrete voltage

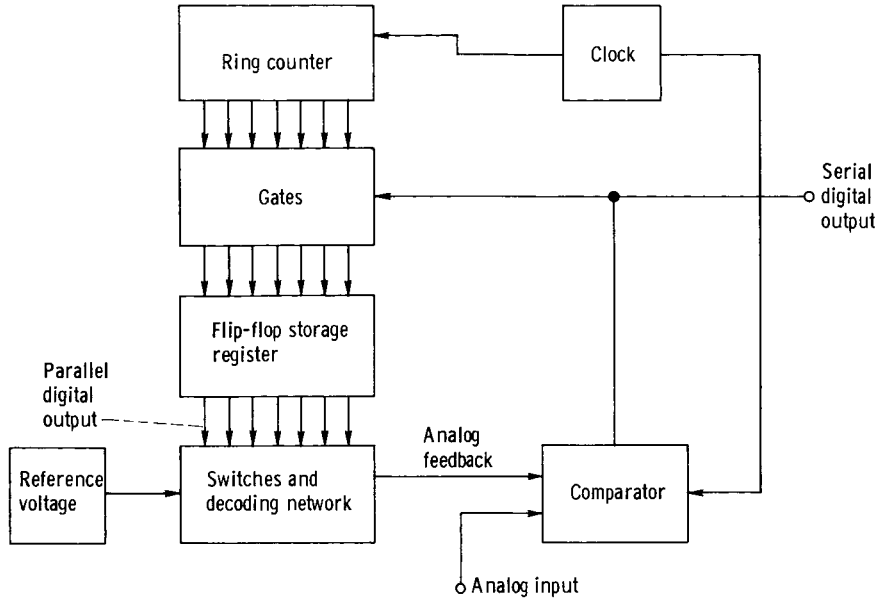


Figure 1. - Elementary diagram for analog-to-digital converter logic.

levels. The analog feedback is generated by summing increments of 1/2, 1/4, 1/8, etc. of full scale in the decoding network; the feedback signal is compared to the input at each step. Whenever the total feedback signal exceeds the input, the comparator directs the storage register to remove the last increment added, and the system then proceeds to the next smaller increment, which is one-half as large. At the end of seven comparisons the feedback signal matches the input to 1 part in 128 at which time the digital representation of the input is read out from the register.

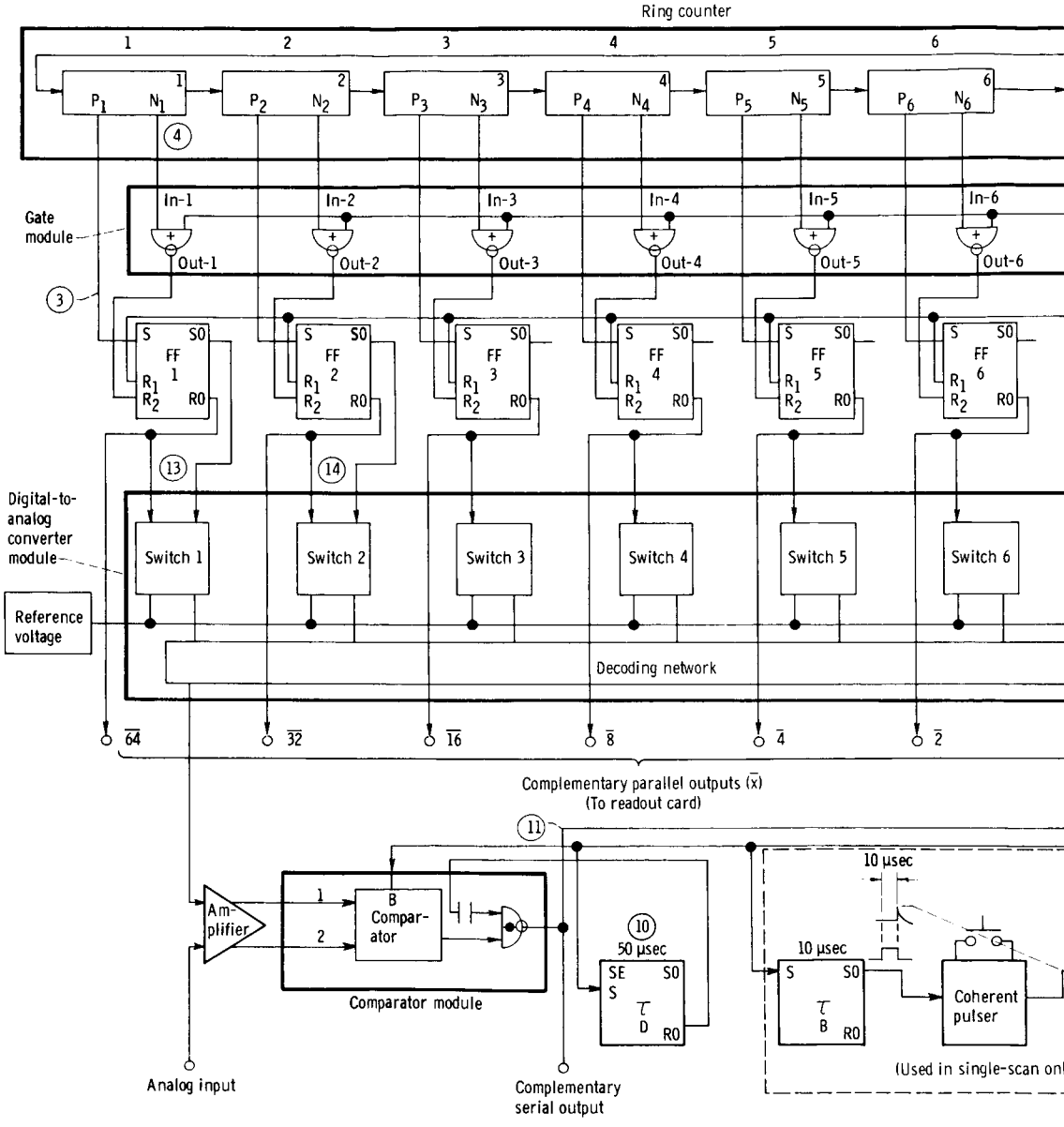
SYSTEM DESIGN

The following sections of this report will show in detail the performance of each element and establish that all of the design goals were met and most of them exceeded.

Converter Operation

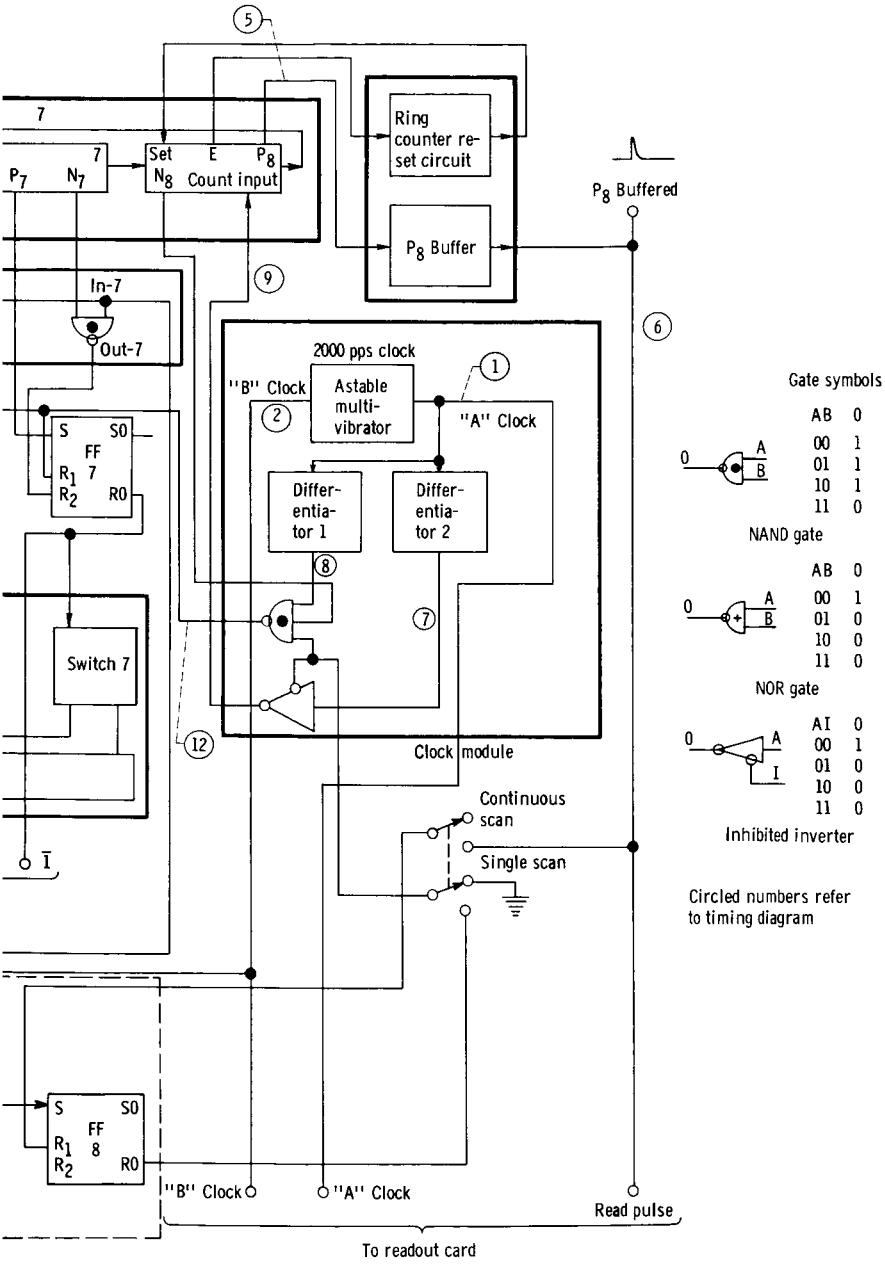
In figure 2 is detailed the logical operation of the converter, which has two modes of operation - single scan and continuous scan.

In the single-scan mode, the converter goes through a complete conversion cycle and stops in the "read out" position. The digital output of the conversion is retained in the flip-flop storage register. The coherent pulser switch must be depressed to initiate each new conversion cycle.



(a) Block diagram.

Figure 2. - Analog-to-digital conve



Gate symbols

AB	0
00	1
01	1
10	1
11	0

NAND gate

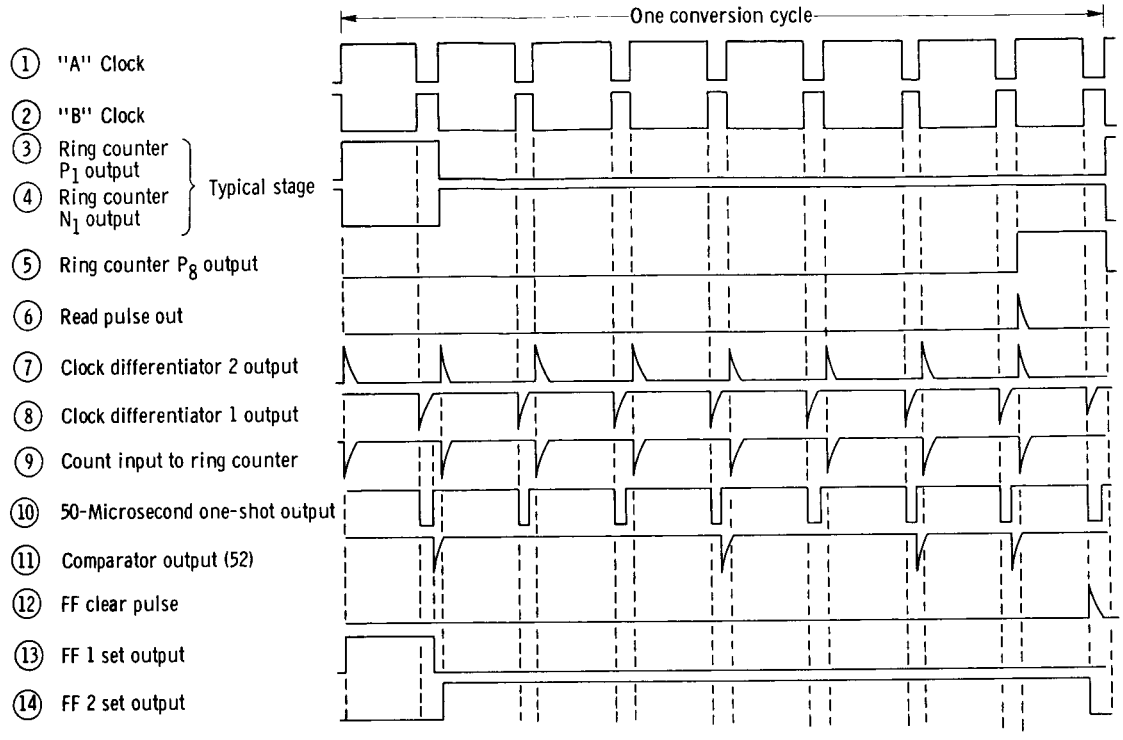
AB	0
00	1
01	0
10	0
11	0

NOR gate

AI	0
00	1
01	0
10	0
11	0

Inhibited inverter

Circled numbers refer to timing diagram



(b) Timing diagram. Converter in continuous-scan mode with digital output of 52.

Figure 2. - Concluded.

In the continuous-scan mode, the ring counter is not inhibited after each conversion cycle so that a new cycle begins on the next "A" clock cycle after the read pulse has occurred. In the continuous-scan mode, the coherent pulser, the 10-microsecond one shot, and flip-flop 8 are not used. The "normal" mode of operation for the purpose of this report was the continuous-scan mode. All of the testing and power consumption measurements were made in this mode.

In this system, logical "1" is approximately supply voltage or 5.0 volts and logical "O" is approximately ground or 0 volts. Leading edge logic is used except where specifically stated.

Basically, the converter compares the input signal to a feedback signal that it generates in a prescribed fashion and determines when the two are equal. The digital number used to generate the feedback signal is the binary representation of the input. A step-by-step description of converter operation follows.

The feedback signal to be compared to the input is generated by the digital-to-analog converter network. It has seven input lines that, when energized, produce an output proportional to the binary value of the input. Thus, energizing the first stage produces an output of one-half full scale; energizing the second stage, one-quarter full scale; etc.

Drive to the digital-to-analog network is provided by a flip-flop register which, in turn, receives signals from a ring counter that programs the sequence of operations in

making a conversion. A 2000-pps clock provides the primary signals to time all logic functions.

A typical conversion starts with all flip-flops reset and the ring counter in the eighth bit position. A pulse from the first or "A" phase of the clock (point 1) causes the ring counter to advance so that the first stage is on (all point numbers refer to fig. 2(a)). The ring counter sets flip-flop 1 (point 3) which, in turn, energizes the first and most significant bit in the digital-to-analog conversion network (point 13). The latter then presents an output of one-half full scale to the amplifier-comparator, which compares this signal to the input. The comparator is energized by the second or "B" clock phase (point 2) that occurs 400 microseconds after "A" clock. Fifty microseconds after "B" clock occurs, sampling of the comparator output is initiated by a delay one shot (point 10). If the feedback signal is larger than the input (input less than one-half full scale), the comparator module produces a pulse (point 11) that is amplified and gated by the gate module. This pulse can only pass through the gate enabled by the ring counter and in this case passes through the first gate stage, resets the first flip-flop, and removes the source of one-half full-scale voltage from the digital-to-analog network. Had the input been larger than one-half full scale no pulse would have been generated by the comparator and the first flip-flop and the digital-to-analog switch would remain on. The ring counter now steps to the second position and the process is repeated, but this time adding in one-half the value of the first stage, or one-quarter full scale. The process continues through the seven stages. If the converter is in the single-scan mode, the clock signal to the ring counter is cut off when it reaches the eighth stage and the converter holds the number until another conversion is called for by energizing the coherent pulser. Alternatively, in the continuous-scan mode the ring counter advances through the eighth stage and starts in at the first again.

In either of these modes of operation there are three different means of reading out the results of the conversion. A pulse occurs at the output of the comparator whenever a bit is to be removed in the conversion process. It is, therefore, the complement of the binary coded number desired. A second means of obtaining the output is by monitoring the states of the flip-flops left on during the conversion cycle. Thirdly, when the conversion cycle is completed a reset signal is fed to all flip-flops from the clock causing a pulse to appear at the output of each flip-flop that remained set during conversion. By the choice of output points it is possible to obtain a serial pulse train, level changes occurring in sequence, or a parallel readout from this converter. Its output is, therefore, compatible with almost any readout system desired.

Readout

No provision for readout has been included in the prototype converter, but an auxil-

iary system was designed and built to give a visual display of the output in decimal form. This readout device is necessarily slow to permit visual readout and, therefore, only samples the converter output approximately once per second. It was designed primarily as a tool for use in checking the performance of the converter. A description of the operation of this device is included in the appendix. A second means of readout is available by displaying the comparator output on an oscilloscope. This method can display each conversion and was also used for performance checking as discussed in the METHOD OF TESTING section.

Operating Speed

Speed of conversion is determined by the clock frequency, which was originally specified at 2000 pps. Eight clock cycles are required for each conversion resulting in a conversion rate of 250 words per second. This is not necessarily the maximum operating rate for a micropower converter using this general operation technique, as will be discussed in the Operating Speed section of the RESULTS section.

Power Supplies

The extremely low-power requirements of this analog-to-digital converter preclude designing separate power supplies for it of any reasonable efficiency. It was assumed that any analog-to-digital converter would necessarily be used with other elements to form a complete data system and that suitable power supplies would be provided for the whole system.

CIRCUIT DESIGN

Digital Circuits

The prime consideration in the design of the logic circuitry of the analog-to-digital converter is low power consumption. Achievement of this aim is accomplished in the circuit design by the use of complementary circuitry for storage and timing and by the use of low-duty cycles in gating circuitry.

Storage of digital data is accomplished in bistable multivibrators (flip-flops). Timing is performed by an astable multivibrator, delay multivibrators (one shots), and a ring counter. Most of these circuits except the ring counter are of the active-load complementary type and similar in basic design. Previous NASA publications (refs. 2 and 3)

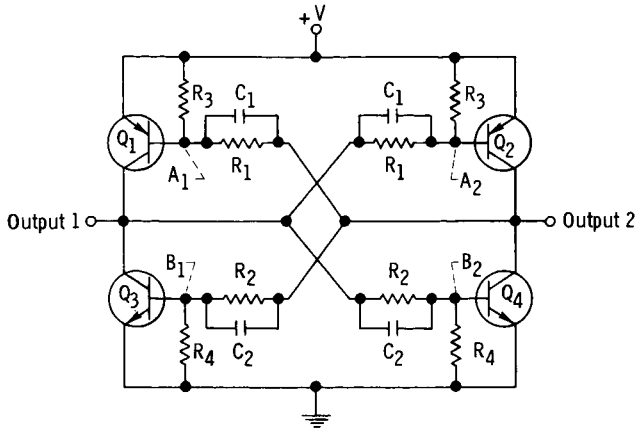


Figure 3. - Basic complementary bistable multivibrator circuit.

discuss the design of these types of logic circuits and the selection of semiconductor devices for them. However, a brief discussion will be included here.

Basic multivibrator circuits. - Figure 3 illustrates the basic complementary bistable multivibrator circuit. In this circuit the load resistors are replaced by PNP transistors that are alternately cut off, which gives high impedance when the lower NPN transistors are saturated or low impedance when the lower NPN transistors are cut off. Triggering can be performed at any of the four transistor bases. A positive pulse at either A_1 or B_1 will cause output 1 to switch off (approach ground level). Alternately, a negative pulse applied to either of these two points will cause output 1 to switch on (approach supply voltage). Conversely, application of pulses to either A_2 or B_2 will have the same effect on output 2.

The advantages of the circuit are low standby power consumption, high efficiency, and low output impedance.

Bistable multivibrators. - The eight bistable multivibrators (flip-flops) used in the system are identical to that shown in figure 4. Resistors R_{11} and R_{12} decrease the shunting effect of the speedup capacitors on the leading edge of the pulse. The 560-picofarad interbase capacitors (C_8 and C_9) couple the bases together in order to decrease transition time. The circuit is triggered by positive-going pulses supplied through standard differentiator circuits. The extra reset input provides a built-in OR function. Total power consumption under normal converter operation is 80 microwatts.

Delay multivibrators. - Two delay multivibrators are used to provide delayed clocking to the coherent pulser and the comparator. Figure 5 illustrates a multivibrator with a delay of 10 microseconds. The purpose of this circuit is to produce a positive-going pulse 10 microseconds after "A" clock has occurred to insure that FF 8 is set after "A" clock. Note, however, that this delay circuit is triggered by a negative-going pulse instead of a positive pulse as in the majority of the other circuits. Thus, "B" clock is used to drive the circuit, and it is triggered at the fall of "B" clock (or rise of "A" clock) to insure proper timing. The delay time is set by C_5, R_6, and C_6.

Figure 6 illustrates a second type of delay multivibrator. This circuit is triggered by a positive differentiated pulse and, therefore, operates on the leading edge of an input pulse. The function of the circuit is to allow the comparator to settle for 50 microseconds before the output is sampled. Timing is controlled by C_4 and R_6. Both delay multivibrators consume 80 microwatts each under normal converter operating conditions.

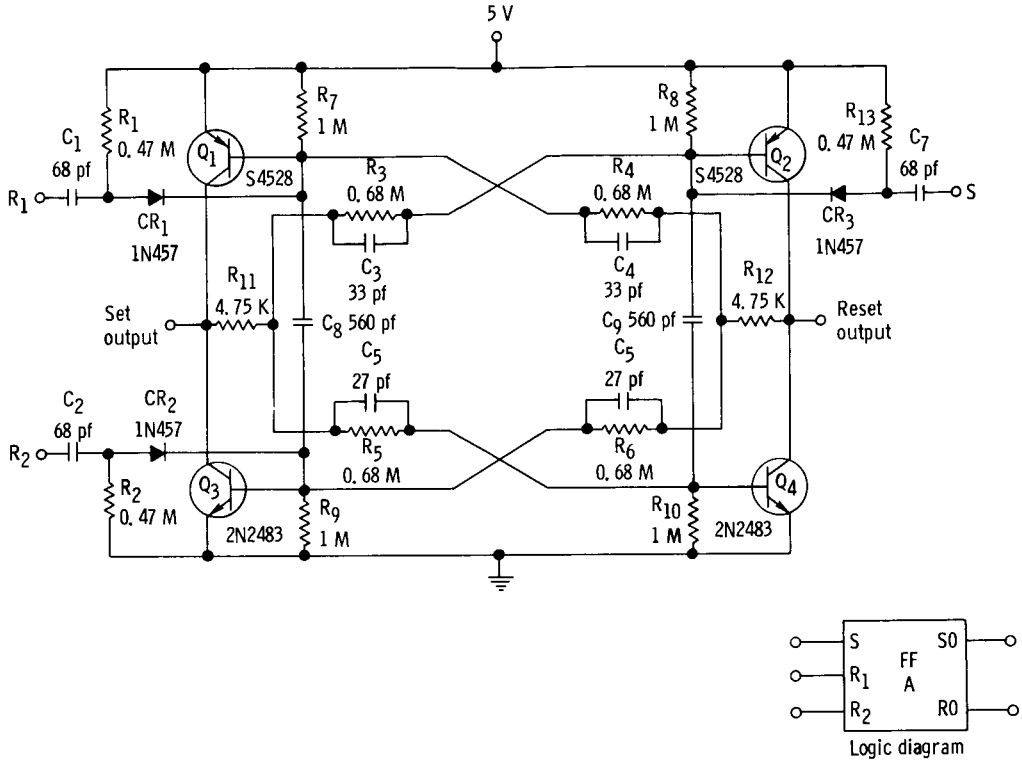


Figure 4. - Set-reset bistable multivibrator (type A).

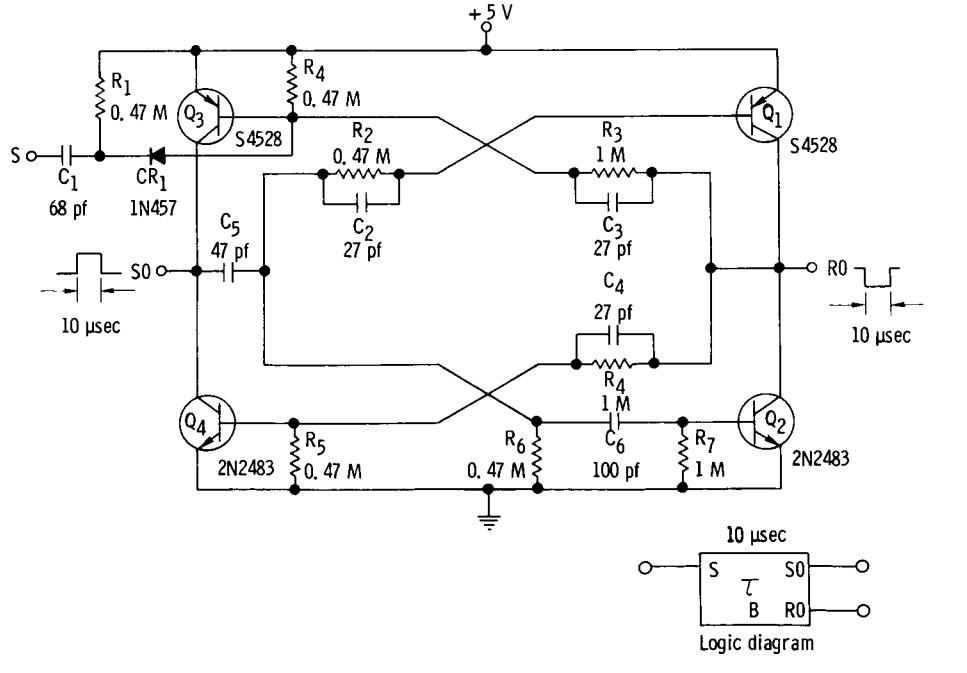


Figure 5. - Ten-microsecond monostable multivibrator (type B).

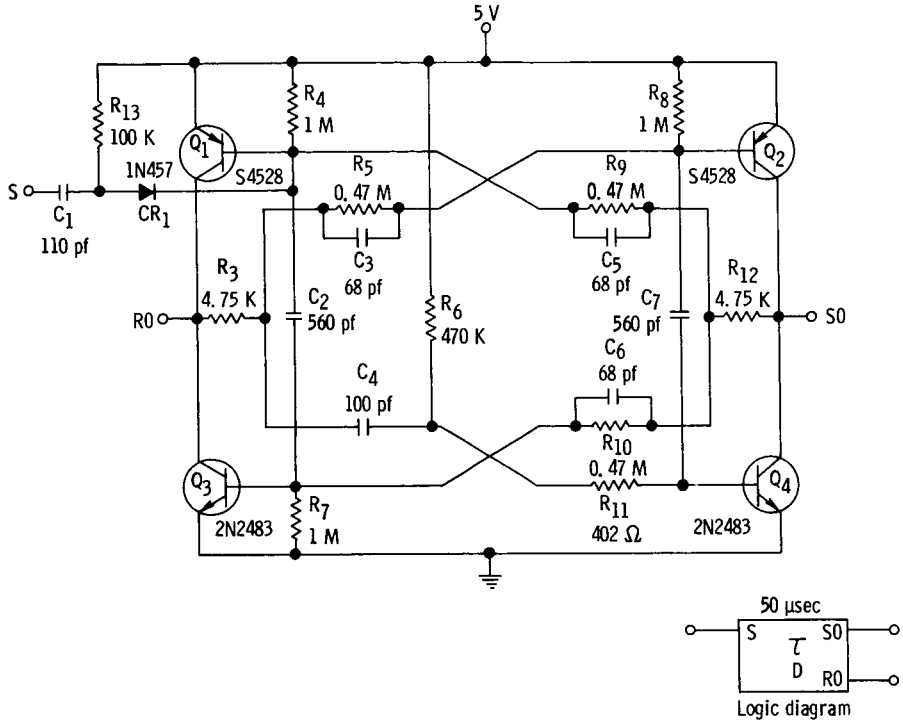


Figure 6. - Fifty-microsecond monostable multivibrator (type D).

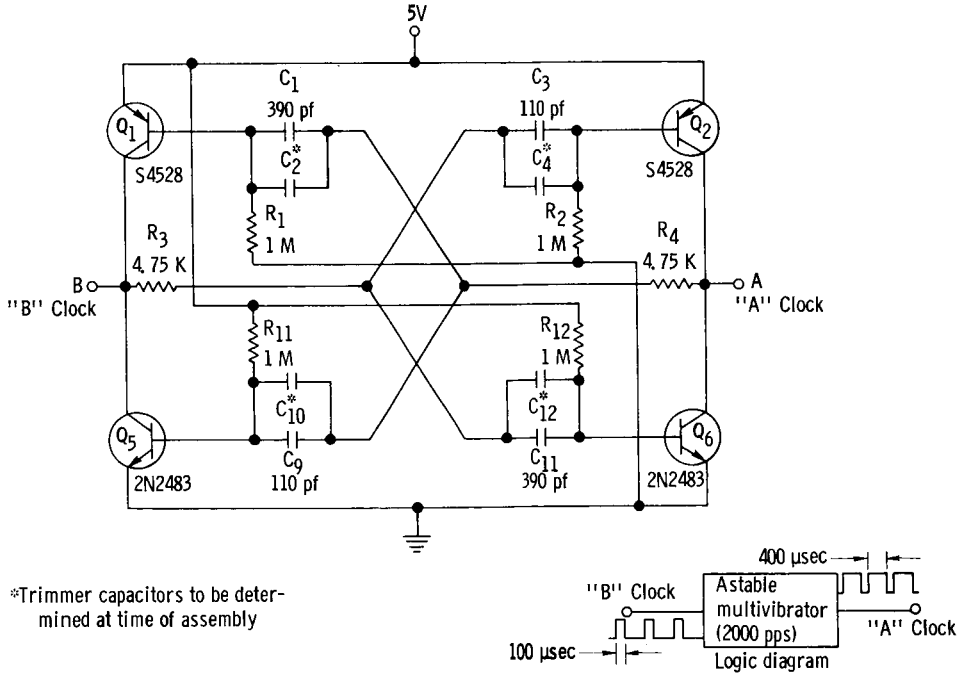


Figure 7. - Astable multivibrator (2000 pps).

Astable multivibrator. - The clock or astable multivibrator is the remaining complementary circuit to be discussed. As can be seen in figure 7, this circuit follows the same design procedure as the bistable and delay multivibrators. The operating frequency, determined by all resistors (except R_3 and R_4) and all capacitors, is 2000 pps. No attempt was made to temperature stabilize the clock frequency as it is noncritical to converter operation. Furthermore, in an actual application, where clock frequency is important, the converter would probably be operated from an external master clock. The clock duty cycle is nonsymmetric with an on-time of 400 microseconds and an off-time of 100 microseconds. On-time is defined as that time when point A is "up" or near supply voltage. This is also referred to as "A" cycle or "A" clock. In the same manner, off-time is defined as that time when point B is up or near supply voltage. This is also referred to as "B" cycle or "B" clock. The duty cycle is nonsymmetric in order to allow the amplifier a relatively long settling time compared to the logic circuitry. The clock module, which includes two gates, requires 300 microwatts of power.

Ring counter. - The only timing circuit which is not of the previously discussed complementary type is the eight-stage ring counter (refs. 4 and 5). Although PNP and NPN transistors are used as paired switches in the circuit (see fig. 8), the circuit is not complementary in the sense that each is an active load for the other because passive load resistors (16.2 K + 23.7 K) are employed in contrast to active load devices. In contrast to other complementary circuits, both transistors in each stage of the ring counter are

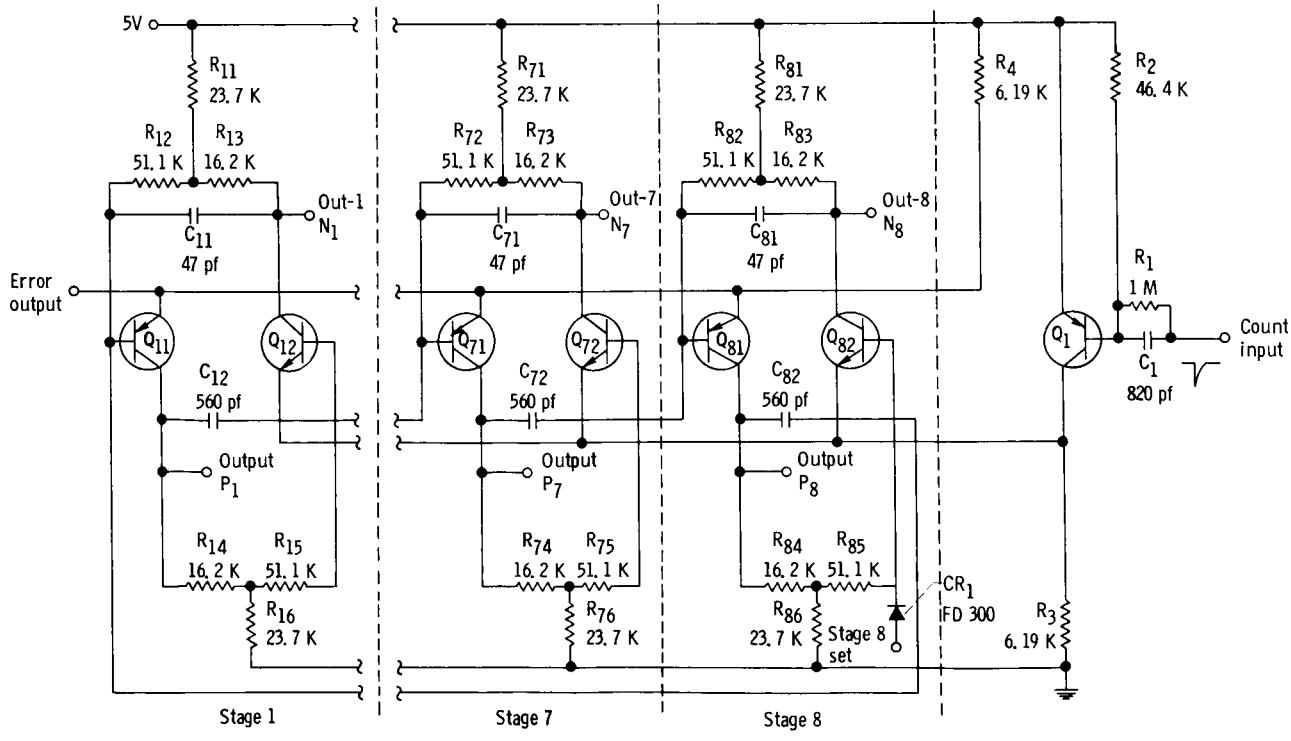


Figure 8. - Eight-stage ring counter. PNP transistors are S4528; NPN transistors are 2N2483.

either saturated or cut off simultaneously.

The circuit shown in figure 8 represents a compromise between three characteristics, which are in order of importance (1) reliable operation, (2) low power consumption, and (3) good output characteristics.

For reliable operation it is important that one, and only one, stage be "on," or conducting, at any given time and that this on condition be reliably transferred to the next stage in the ring upon the application of a negative pulse to the count input. Possibility of more than one stage conducting at a time is eliminated by inclusion of R_3 and R_4 in the common emitter lines. Transistor biasing is set so that with only one stage conducting the voltage drops across R_3 and R_4 are insufficient to prevent the transistors from going into saturation. If two or more stages attempt to conduct, however, the currents through R_3 and R_4 cause voltage drops across them which, in turn, drive the emitter lines toward cutoff preventing a second pair of transistors from turning on.

The PNP input buffer stage supplies positive pulses to the NPN emitters temporarily cutting off all stages and transferring the count to the next stage by charge transfer from the coupling capacitor of the stage previously on. The pulse out of this stage must be long enough to perform the transfer reliably but shorter than the coupling circuit time constant for proper circuit operation.

Because of the special biasing required, the ring counter does not lend itself to the active load approach to micropower. Therefore, a careful tradeoff must be made between low power and output impedance. Thus, the loading was carefully determined on each stage. From this study the resistor and capacitor values were chosen to yield reliable operation under load over the temperature and voltage range required and yet consume the lowest possible power. Also, transistor current gains were matched (±20 percent) to increase reliability.

The ring counter is one of the more critical digital circuits in the system. Maximum capacitive loading on the "P" or positive-going outputs is approximately 200 picofarads and on the "N" or negative-going outputs is 70 picofarads. If loads greater than the input of a flip-flop are to be driven by the ring counter, buffer amplifiers must be employed, as in the case of the P_8 or "read" buffer. Total power consumption of the ring counter under load and normal operating conditions is 1.1 milliwatts.

Ring counter reset circuit. - The ring counter is stable in the all-zero state, but this is an undesirable state. Therefore, its occurrence, either at initial power turn-on or through random system failure, must be detected and corrected. The circuit in figure 9 monitors the ring counter PNP emitter line. Normally this line is approximately 0.6 volt below supply voltage. The transistor Q_1 in the reset circuit is biased so that the 0.6-volt differential is sufficient to keep it saturated, which in turn keeps Q_2 cut off. However, when the all-zero state occurs, the emitter line goes to supply voltage cutting off Q_1 and turning on Q_2. The collector voltage of Q_2 is applied to the ring counter

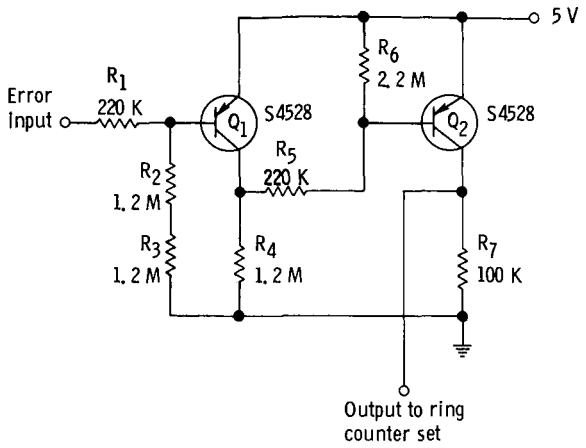


Figure 9. - Ring counter reset circuit.

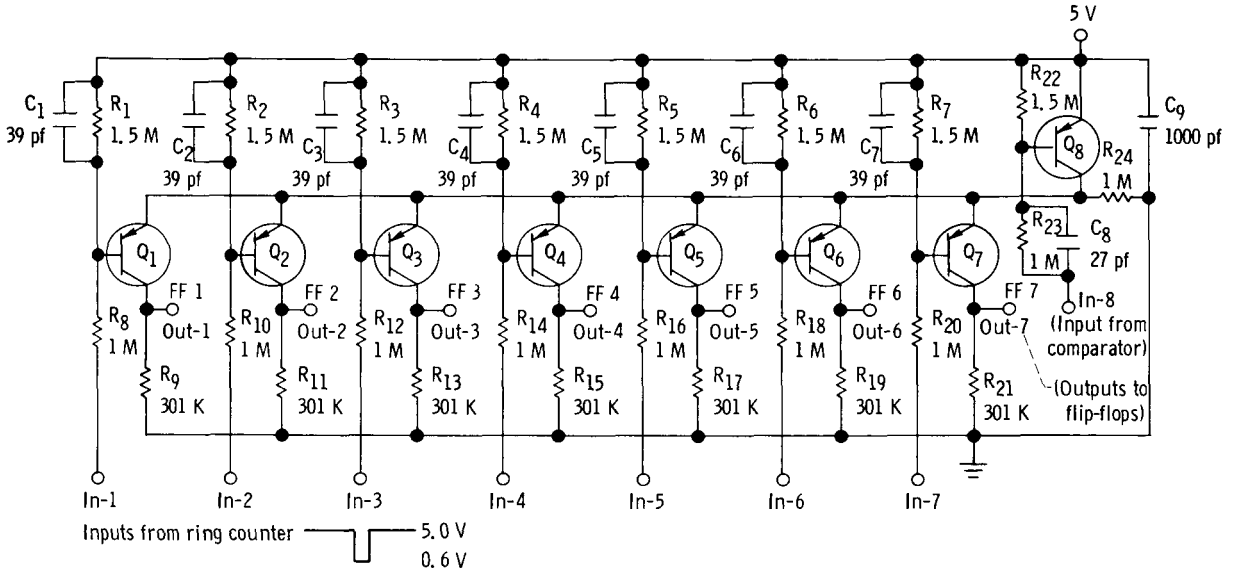


Figure 10. - Storage register gates All transistors are S4528.

through CR_1 to the base of Q_{82} causing stage eight to be set. Power consumption of the reset circuit under normal operation is less than 20 microwatts.

The gating and pulse buffer circuitry employs standard passive load techniques and low-duty cycles. It was found, by judicious use of both NPN and PNP transistors, differentiating circuits, and duty cycles of 2 percent and less, that power consumption comparable to special complementary gates could be achieved at a parts saving. However, because of the larger time constants inherent in conventional passive load logic, the previous statement is true only if the clock rate is relatively low and circuit loading is minimal.

Storage register gates. - In general, NAND and NOR gates are used throughout the converter with one input differentiated to yield low-duty cycles. The gate module of figure 10 is an example of NOR logic. Transistors Q_1 through Q_7 share one common upper

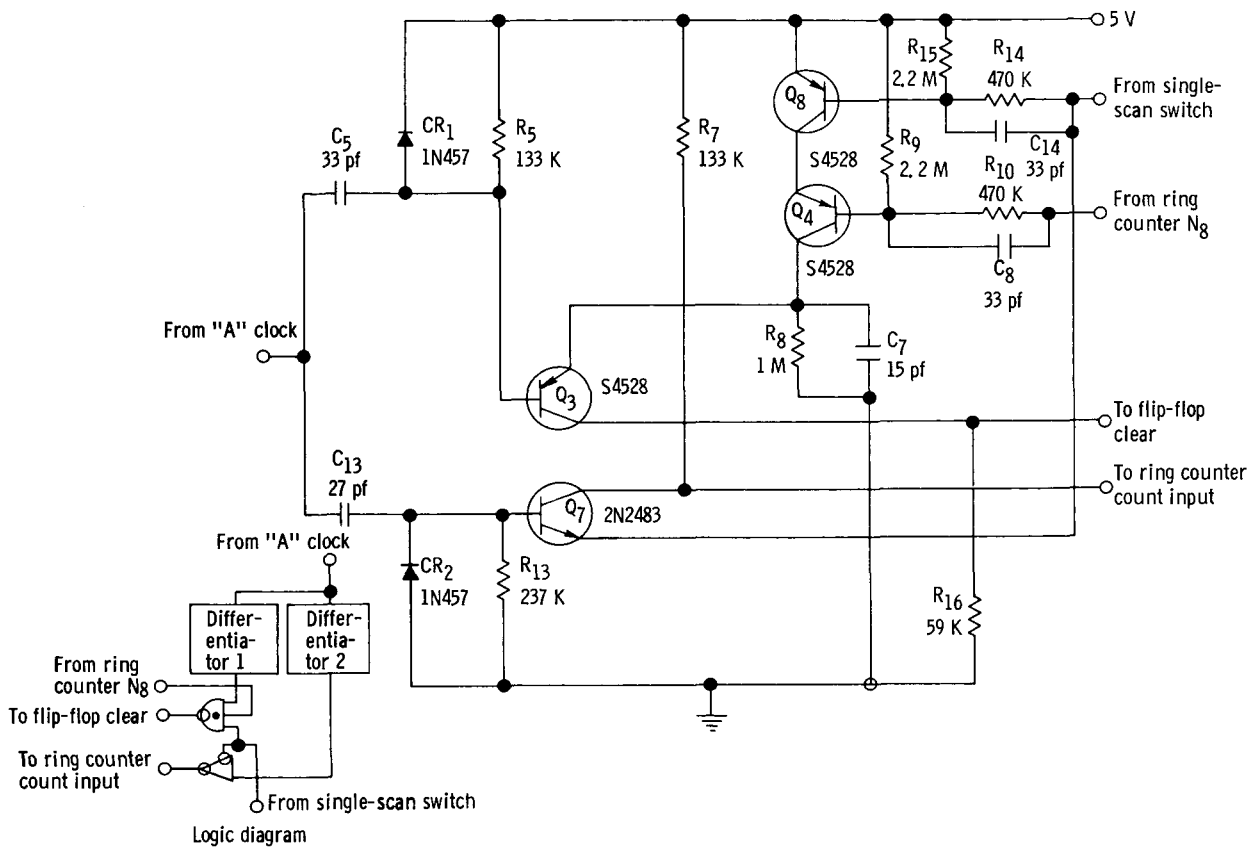


Figure 11. - Clock gates.

transistor Q_8, which is clocked by a narrow pulse from the comparator. Transistors Q_1 through Q_7 are connected through 1-megohm base resistor to the "N" outputs of the ring counter, so that only one transistor can be conducting at a time. Total power consumption under normal operating conditions is 30 microwatts.

Clock gates. - The clock gates (fig. 11) have the function of producing flip-flop register "clear" pulses and ring counter drive pulses. Transistors Q_8, Q_4, and Q_3 with load resistor R_{16} form a three input NAND gate to produce the clear pulses. Note that the input to Q_3 is derived from the trailing edge of "A" clock through a differentiator. Load resistor R_{16} is kept low to provide sufficient energy to reset seven flip-flops simultaneously, yet the duty cycle is kept short so as to minimize power consumption over the cycle.

Transistor Q_7 supplies negative-going differentiated "A" clock pulses to step the ring counter. A positive input from the single-scan switch inhibits the circuit. The gate structure is that of an inhibited inverter, which has the same truth table as a two input NOR gate.

The clock gates are packaged in the same module as the clock (astable multivibrator). Total power consumption of the whole module under normal conditions is 300 microwatts.

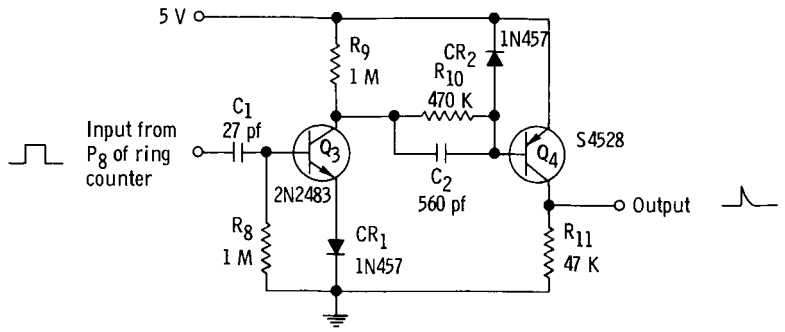


Figure 12. - P_8 buffer circuit.

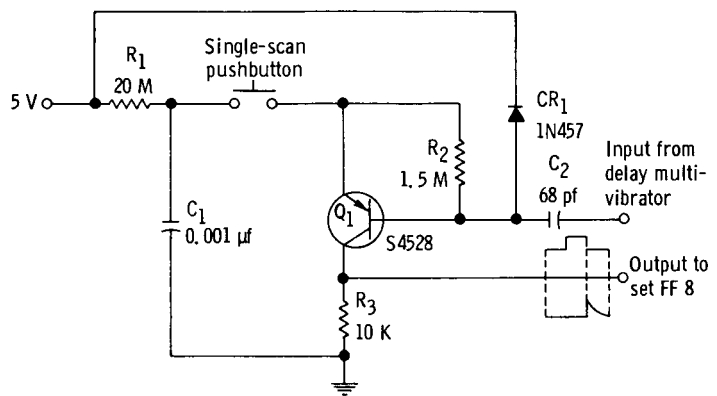


Figure 13. - Coherent pulser.

Buffer amplifier. - The P_8 buffer (fig. 12) provides a pulse output when the eighth stage of the ring counter is turned on. The purpose is to provide a "conversion complete" or "read" pulse to peripheral equipment. Normally both transistors Q_3 and Q_4 are cut off; however, when ring counter P_8 goes positive, the differentiated signal momentarily causes Q_3 to conduct, which, in turn, causes Q_4 to conduct. A positive pulse is provided from a relatively low-impedance source (47 K). Total power consumption is 27 microwatts under normal operating conditions. This circuit is packaged in the same module as the ring counter reset circuit.

Coherent pulser. - The coherent pulser (fig. 13) supplies a positive pulse to set FF 8 and initiate one conversion cycle each time the single-scan button is depressed. However, the pulse is clocked on 10 microseconds after "A" clock. When the momentary pushbutton switch is depressed and when Q_1 is turned on momentarily by the differentiated trailing edge of the 10-microsecond square wave, the energy stored in C_1 discharges through Q_1 causing a positive spike at the output. Once C_1 has discharged, the switch must be released to allow C_1 to recharge through R_1. The recovery time is approximately 50 milliseconds. Power consumption of this circuit is negligible.

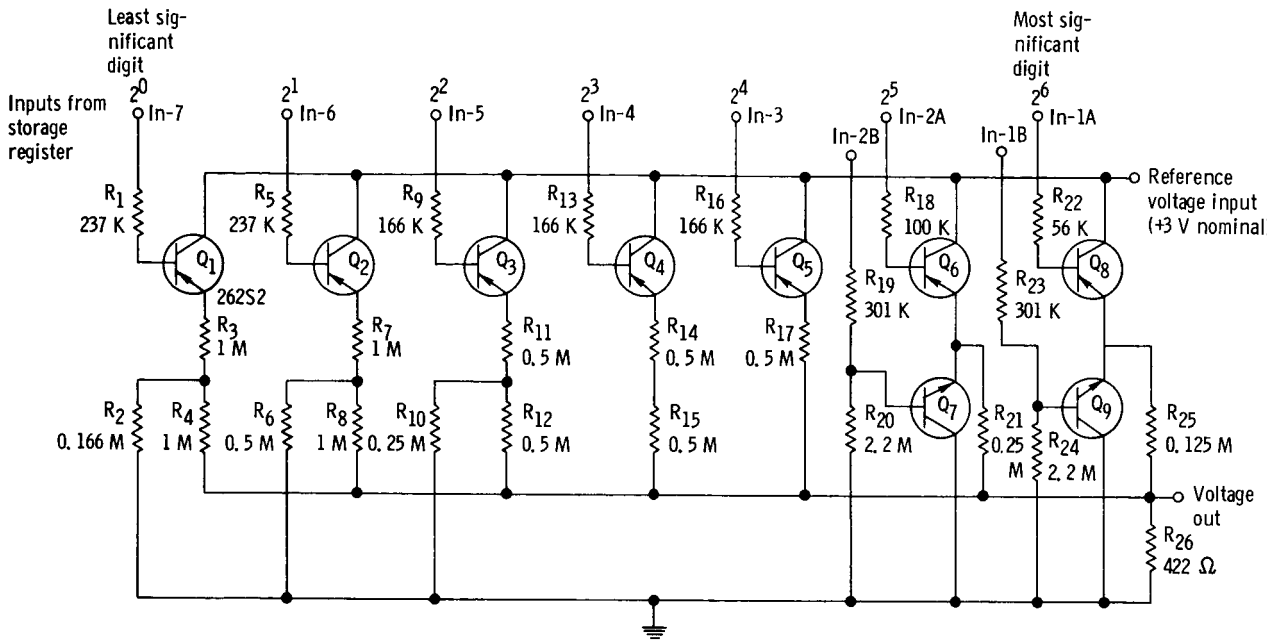


Figure 14. - Digital-to-analog converter network. PNP transistors are 262S2 (select 2N941); NPN transistors are selected 2N2222.

Analog Circuits

In order to meet the target specifications (error less than 1 percent of full scale over 100° C temperature range) great care had to be taken to preserve system accuracy. However, power consumption must be kept minimum in order to achieve the goals of the project.

Digital-to-analog converter network. - The digital-to-analog converter network (fig. 14) provides an analog voltage from 0 to 20 millivolts proportional to the digital seven-bit word currently stored in the register. The standard ladder resistor technique was discarded in favor of a current summing technique because of the higher power consumption of the ladder network. The PNP transistors, used in the inverted configuration, are driven from the complementary outputs of the storage register flip-flops so that a 0 voltage level turns on the transistors and a voltage of 5 volts cuts them off.

When a particular stage n ($1 \leq n \leq 7$) is turned on, a voltage of $20/2^n$ millivolts is applied to the output (no load). Stages one and two (two most significant digit stages) are returned to ground through NPN transistors when these stages are off. This is not done in remaining stages, however, at a cost of a small amount of accuracy in the form of a varying output impedance but at a saving of power.

All transistors are used in inverted form (i. e., collector and emitter interchanged)

because the inverted saturation voltage $V_{EC, SAT}$ is 1 to 3 millivolts, whereas used in the normal fashion $V_{CE, SAT}$ is approximately 100 millivolts. A 3-millivolt difference in the reference can be neglected in relation to other system errors as the maximum error introduced is only 0.1 percent. Even this small error can be partially compensated for by adjusting the reference voltage.

Note that divider networks are utilized in the three least significant digit stages in lieu of 2-, 4-, and 8-megohm resistors, respectively. This was done as resistors over 1 megohm in the physical sizes and tolerances necessary were not available. The output impedance of the network is 420 ohms. This impedance is of the same order of magnitude as that of the sensors, which will supply signals to the analog-to-digital converter under normal operations.

The circuit depicted is linear to ±0.25 percent of full scale (20 mV) when loaded with 0.2 megohm or greater. Average power consumption from supply (storage register) under normal conditions is 80 microwatts. Worst case power consumption from reference supply is 300 microwatts.

Comparator-amplifier system. - The output of the digital-to-analog converter is compared to the input by an extremely sensitive, high-gain comparator that is actually built out of two cascaded elements. The first is a low-drift direct-current differential amplifier followed by a pulsed comparator circuit. Although the amplifier precedes the comparator in the electrical circuit, the latter will be discussed first because the amplifier trimming and operation depend on the comparator characteristics.

Comparator: The comparator with associated NAND gate (fig. 15) is essentially a polarity sensing device. It accepts a true differential voltage from the direct-current amplifier and provides sufficient common-mode rejection so that its operation is not degraded by a 0.25-volt change in common-mode voltage.

In operation, the differential signal from the amplifier is applied to the bases of the lower transistors through special networks. The amplifier and comparator signals are allowed to settle for several hundred microseconds after a new input is applied and the comparator is then energized by a positive pulse derived from "B" clock. The comparator is basically a current-mode bistable multivibrator and will assume a zero or one output state depending on which transistor base, Q_{1a} or Q_{1b}, is receiving more current. Fifty microseconds later the output is sampled by the NAND gate and a negative output pulse is provided when the voltage at input 1 is greater than that at input 2.

The input networks of the comparator provide both limiting and decoupling functions. Capacitors C_{11} and C_{12} serve to roll off the frequency response of the system thereby reducing high-frequency-noise pickup. Resistors R_{22} and R_{23} serve to decouple the amplifier from the comparator input and thereby prevent amplifier oscillation. Diodes CR_5 and CR_6 prevent the comparator inputs from going appreciably positive. Without the diodes, if input 2 of the comparator is allowed to go sufficiently positive, as would occur

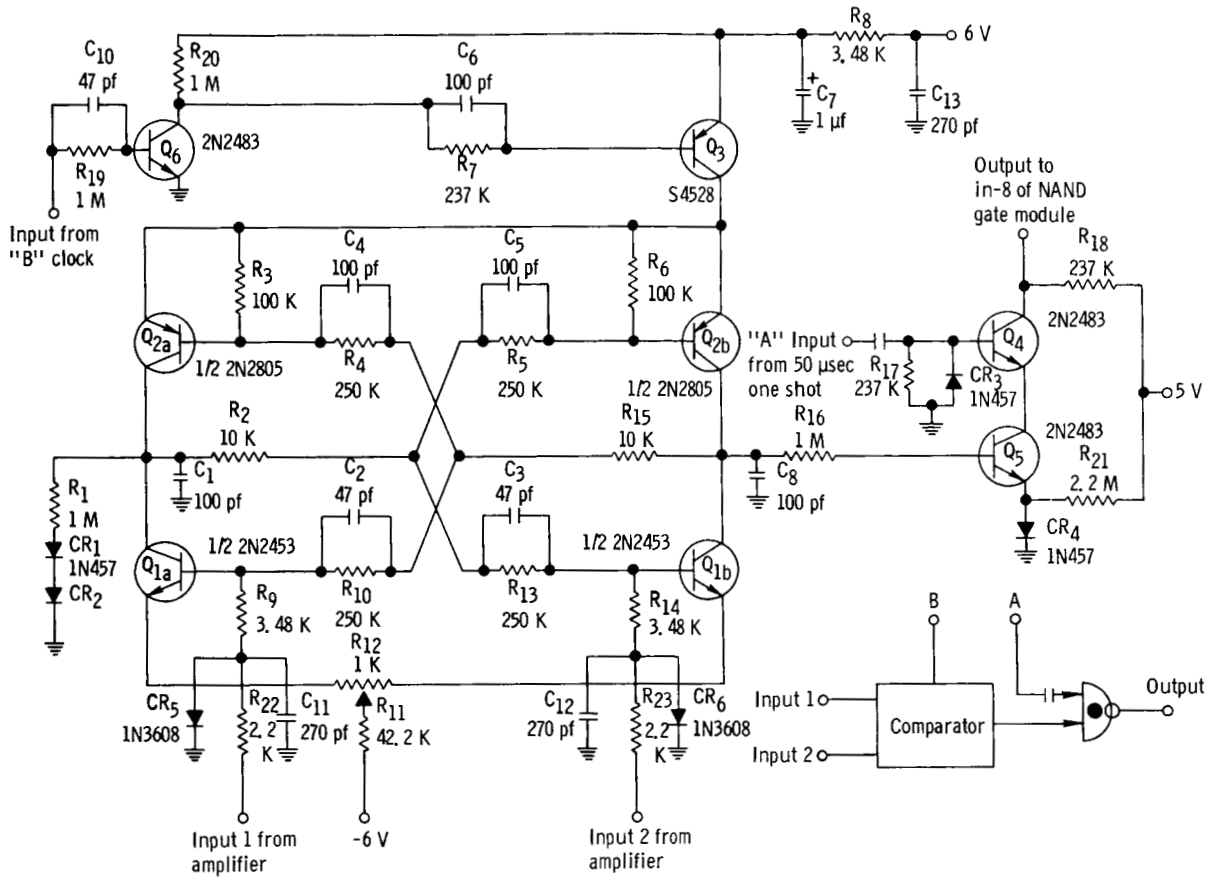


Figure 15. - Comparator with NAND gate.

during amplifier saturation, the collector voltage of Q_{1b} cannot go sufficiently negative during the time that it is saturated to keep Q_5 cut off. The result is that pulses are produced by the comparator when none should occur. These pulses, in turn, turn off the register flip-flops and lower the feedback voltage to the amplifier. The amplifier would be driven further into saturation, the action being regenerative. The effect is that if an analog input voltage near or greater than full scale were to be applied, the converter would read zero or a small number. Diodes CR_5 and CR_6 prevent this from happening.

Very low hysteresis and shift of trigger point with temperature are required of the comparator circuit. It is, therefore, designed for nearly perfect symmetry between the two sides forming the multivibrator. Closely matched dual transistors were used for both the PNP and NPN stages of the multivibrator and resistor R_1 and diodes CR_1 and CR_2 were added to the unused output as a dummy load to maintain balance. Final balancing is accomplished with potentiometer R_{12} located in the emitter circuits of the NPN transistor pair.

Hysteresis of the circuit is less than 3.0 millivolts, and temperature drift is approximately 7 millivolts over the temperature range of -20° to $+80^{\circ}$ C. When referred to the input of the differential amplifier this drift appears as less than 1 microvolt per $^{\circ}$C.

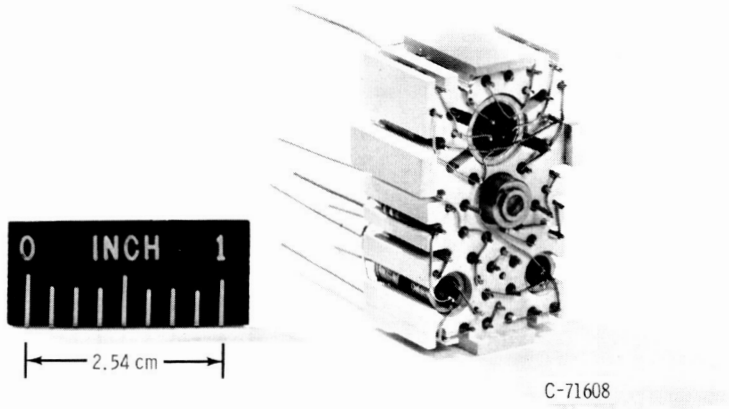


Figure 16. - Comparator module.

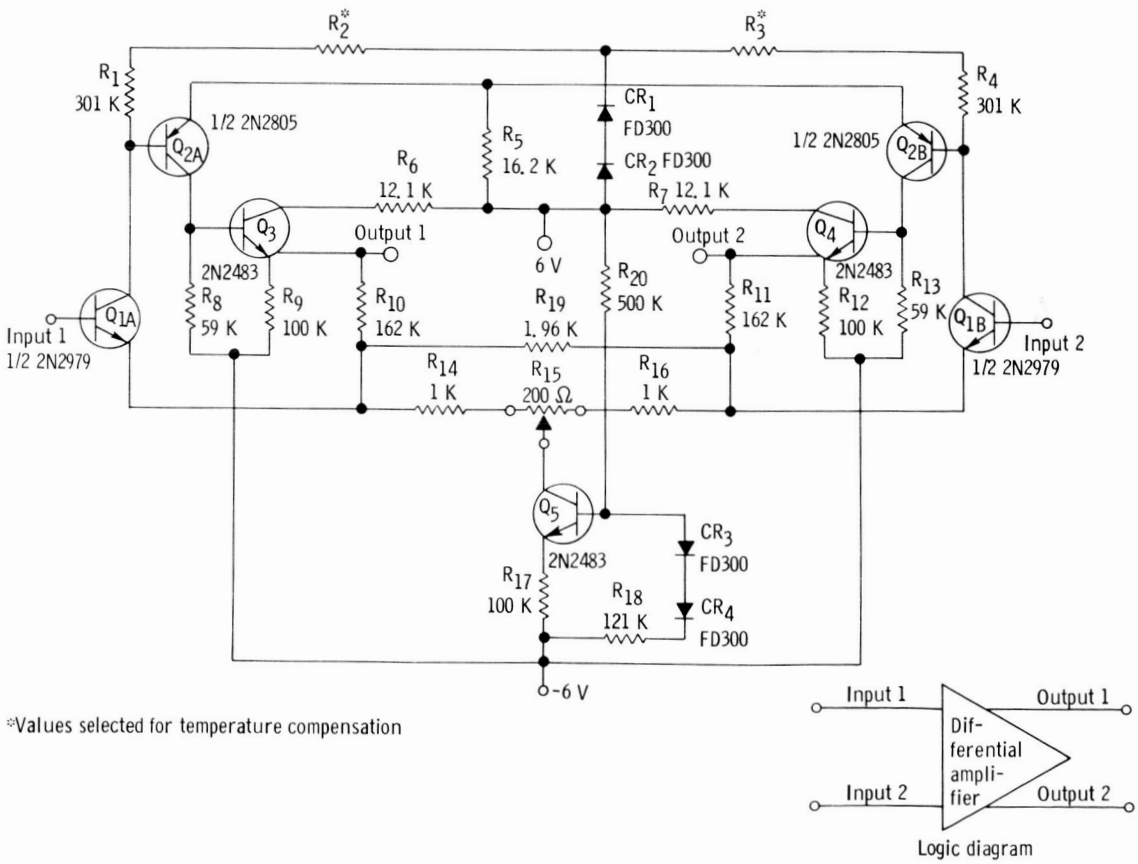


Figure 17. - Low-level differential amplifier.

Power consumption of the comparator is 1.2 milliwatts at 25° C.

In order to reduce thermal gradients through the module, the comparator (as well as the amplifier) was constructed by using a highly thermally conductive boron nitride nesting jig (see fig. 16).

Amplifier: The low-level differential amplifier employed to amplify the difference between the input to the analog-to-digital converter and the feedback voltage from the digital-to-analog network is shown in figure 17. It has both a differential input and a differential output, which considerably simplify its design.

To meet the design specifications the amplifier, when considered by itself, must have a thermal drift coefficient of less than 0.5 microvolt per °C. This rather severe requirement along with that of very low power consumption eliminates chopper stabilization as a method of achieving low drift. Semiconductor choppers have drift characteristics worse than the specification, and electromechanical choppers are not feasible because of both short life and high-power requirements. It was, therefore, necessary to use an amplifier without external stabilization and rely on various means of temperature compensation to provide the desired performance.

Essentially, the circuit consists of two common-emitter stages to provide voltage gain followed by a common-collector stage to provide low output impedance. Transistor Q_5 provides a constant current source to the emitters of Q_{1a} and Q_{1b} for high common-mode rejection and first-stage current stability. Overall negative feedback is provided by resistors R_{10} and R_{11}.

Silicon diodes CR_1 through CR_4 provide some amount of temperature compensation. High-quality metal film resistors are employed throughout the amplifier to reduce thermal drift. In addition, measures to reduce thermal gradient throughout the circuit include the use of matched dual transistors Q_1 and Q_2 and the use of highly thermally conductive boron nitride as a nesting jig as in the comparator.

The specifications for the direct-current amplifier are as follows:

Open-loop voltage gain, db	62
Closed-loop voltage gain, db	48
Maximum input current at -20° C, nA	120
Output impedance	approx. 3 kΩ differential
Frequency response	3 db down at 60 kc
Thermal drift (referred to input), μV/°C	0.25
Common-mode rejection (balanced 500 Ω source at 1 kc), db	74
Overload recovery (0.25-V input), μsec	5
Power requirement	
At 6V ± 1 percent, mA	0.46
At -6V ± 1 percent, mA	0.40
Total power consumption, mW	5.2

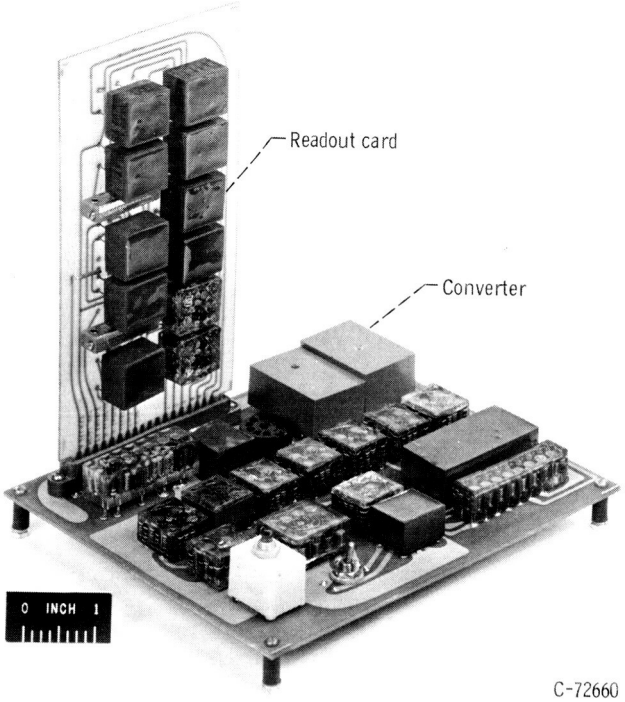


Figure 18. - Analog-to-digital converter with readout card.

These specifications are for the amplifier as built and tested apart from the analog-to-digital converter but with simulated load. When the whole system was breadboarded, it became evident that other components of the system had appreciable temperature drifts. Of these, the comparator was the worst offender. In order to correct for this system drift, which was approximately linear with temperature, it was decided to introduce an equal but opposite drift in the differential amplifier. This was relatively easily accomplished by trimming the first-stage collector resistors with R_2 and R_3 as was done to eliminate drift originally. This proved very effective, as will be shown, since the drift obtainable from the differential amplifier was correspondingly linear.

The complete analog-to-digital converter with readout card is shown in figure 18. The nine pin socket provides input-output connections to the system.

METHOD OF TESTING

Operational and stability tests were made with the setup shown schematically in figure 19. In essence the procedure was to digitally program a scaled analog voltage and apply it to the input of the analog-to-digital converter. The converter digital output was then compared to the programer setting. The digital programer was such that tenths or even hundredths of a digit could be supplied to the converter. In this way exact change points between digits could be determined and deviation over temperature and supply voltages determined.

A digitally programable power supply, which produced voltages from 00.000 to 99.999 volts with 0.05-percent accuracy, provided the input to the analog-to-digital converter through a voltage divider. The divider resistors were chosen such that 12.7 volts from the programable power supply would provide 20.0 millivolts (full scale) to the converter. Thus, a 5.2-volt input to the divider would cause the analog-to-digital converter to display the number 52. The parallel binary output of the analog-to-digital converter

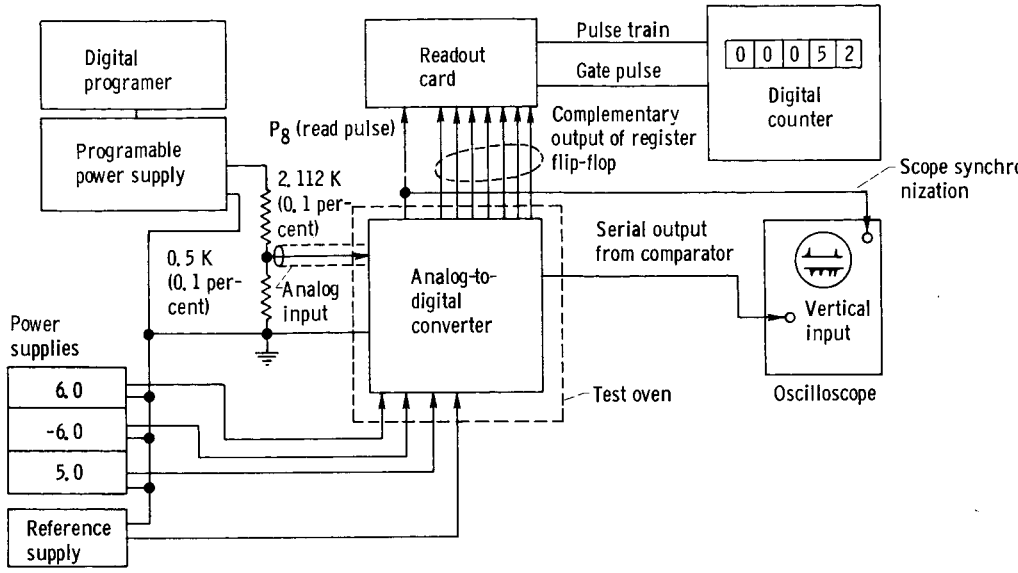


Figure 19. - Setup used to check analog-to-digital converter accuracy.

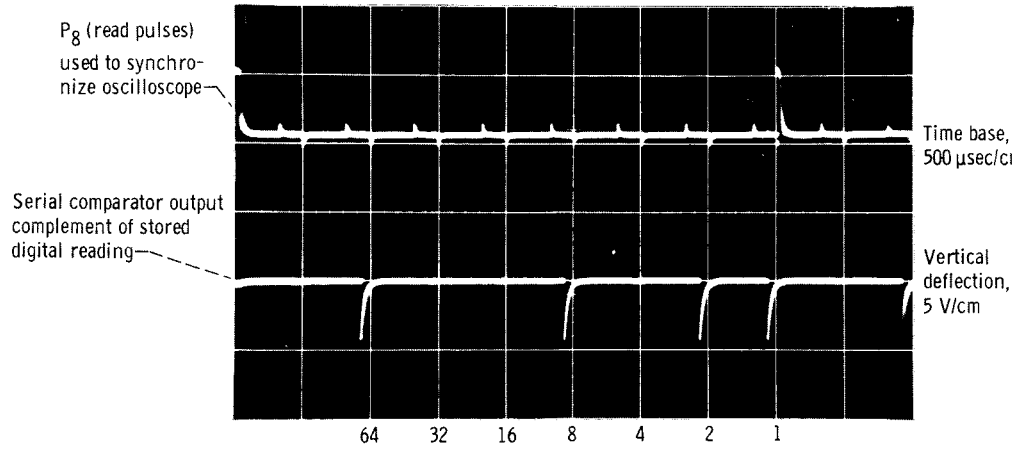


Figure 20. - Serial comparator output.

was then sampled by the readout card (see appendix) and displayed in decimal form on a digital counter. Since the minimum display time of the digital counter was approximately 0.5 second, approximately 1 of every 125 analog-to-digital conversions was sampled.

The converter count was also monitored by observing the comparator gate output on an oscilloscope (see fig. 20). The negative-going pulses on the lower trace represent the reset pulses to the flip-flops. The pulse train therefore displays the complement of the number currently being converted. The complement of a binary number X is defined as $\overline{X} = 2^n - 1 - X$, where n is the word length. In this case $n = 7$ so that $\overline{X} = 127 - X$. The number displayed in the figure is $32 + 16 + 4$ or 52. Since every conversion was displayed on the oscilloscope, a random error (or wrong count) was observed as a flicker in the trace.

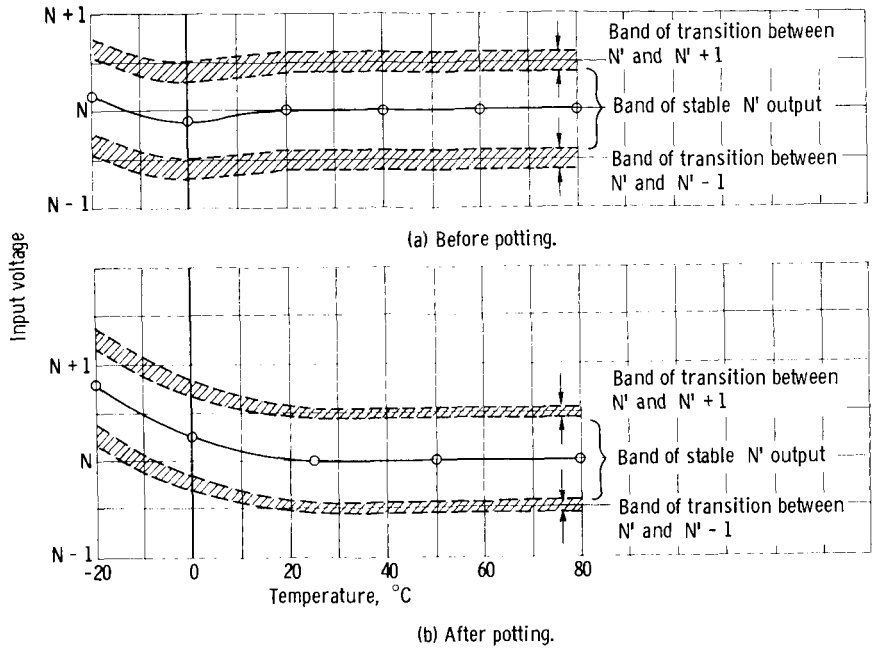


Figure 21. - Converter input-output characteristic as function of temperature.

The procedure for checking the converter was as follows: (1) stabilize the converter at a given temperature in a test oven for 15 minutes and at a given set of supply voltages; (2) program in various sample counts from 0 to 127 (0 to 20 mV); (3) vary the one-tenth count (hundredth volt digit on the programer) until flicker was observed on the comparator trace for each sample; and (4) determine the "aperture" for each count from step 3.

Figures 21(a) and (b) are plots obtained by using the previous procedure. The vertical axis represents an input from the digitally programable power supply. The N is any number from 0 to 127 and the 10 divisions from N to N + 1, or from N - 1 to N, represent settings in tenths of a count from the programable power supply. The N + 1 represents the next higher integer over the given number N and N - 1 the next lower integer. The aperture band N' represents the area of those conditions of temperature and analog input under which a stable digital output of N results. The two cross-hatched transition areas are those in which the count is indecisive between N and N + 1 (or N - 1 and N). The solid line represents the center of the aperture. Ideally, the solid line should coincide with the analog input N for all values of temperature and the transition bands should approach zero width. Deviation of the solid line with temperature represents thermal drift. The wider the transition bands, the less the system resolution. Comparator hysteresis, decreased gain, and noise all contribute to an increased transition band width.

The data represented on figure 21(a) were taken after the system had been completed but before the amplifier had been encapsulated. It was obtained by adjusting the thermal drift of the direct-current amplifier to minimize total system error. Because the ampli-

fier was trimmed as closely as possible when operating with the specific test setup used, compensation was automatically made for drifts that might be a function of the input such as that due to changes of input current requirement with temperature. It represents the ultimate accuracy attainable with this converter.

The amplifier was then encapsulated and the testing procedure repeated. Figure 21(b) illustrates the results. The chief difference in the two sets of curves is the deviation of three-fourths count at -20° C on the graph taken after potting. The results will be discussed in greater detail in the next section of this report.

RESULTS

It will be shown in this section that the original target goals were, for the most part, conservative when compared to the performance actually attained.

Power Consumption

The most important characteristic of this analog-to-digital converter is its extremely low power consumption. The current drain and power required from each of the supplies as well as the total power requirement are tabulated in table I.

Power required from the 5.0-volt logic supply and the -6.0-volt supply is relatively constant. The same is true of the 6.0-volt supply but only for inputs between 0 and 20 millivolts. If a negative analog input voltage is applied, an analog input greater than 20 millivolts is applied, or if the converter is operated in the single-scan mode and the analog input is varied so that the system is not allowed to balance, then the resulting unbalance will drive the direct-current amplifier into saturation. Under this condition the amplifier will increase the current drain on the 6.0-volt supply to a maximum of 830 microamperes. Since any of these conditions constitute abnormal operation, the figure given in the table is the maximum that will occur in normal operation. Similarly, the current drain and power requirements on the reference supply are given for the worst condition, which corresponds to digitizing a full-scale voltage. If the inputs to the analog-to-digital converter were random, the actual current drawn from the reference supply would approach half that shown.

TABLE I. - CURRENT REQUIREMENTS AND POWER CONSUMPTION OF ANALOG-TO-DIGITAL CONVERTER

Supply, V	Current, μA	Power, mW
5.0 (logic)	490	2.45
6.0	550	3.30
-6.0	490	2.95
3 (nominal reference)	230	.70
	Total	9.40

Operating Speed

The fact that the digitizing rate of this converter is relatively slow does not indicate a fundamental limitation. All of the digital elements of the converter, with the exception of the ring counter, could be easily modified to operate at 10 times the present rate. The same is true for the analog elements; in fact, the speed of response of the amplifier, and to a lesser extent the comparator, is in excess of the minimum required for this converter. Only one element, the ring counter, would require a major change. Because of power requirements as well as performance, it would be desirable to replace the ring counter with some other device.

Power requirements for a converter capable of faster operation would necessarily be higher. All of the micropower circuits involved exhibit a speed-power tradeoff, but it is not necessarily linear. It is expected that power consumption measured on the basis of power per conversion would actually decrease as speed is increased until approximately a 500 000 pps clock rate is reached. An increase in conversion rate by a factor of 10 over the present system could probably be achieved without more than doubling the power required.

Weight and Volume

Weight and volume were considered to be of secondary importance in designing this converter. One of the reasons for this attitude is the rapid progress being made in the various techniques of microminiaturization. The techniques used to build the modules were close to the best available at the inception of this study; however, since then smaller components and better fabrication techniques have become available so that a large reduction in weight and volume can now be achieved in the modules.

The achievement of a total weight and volume of 283 grams and 134 cubic centimeters, respectively, for the prototype converter is good when considering the techniques used in the construction. These actual figures are of value only for comparison purposes as it would be possible to considerably better them for any flight system constructed today.

Thermal Effects

All electrical goals were also met. Satisfactory performance was obtained over the design temperature range of -20° to $+80^{\circ}$ C, and there was no indication of imminent failure at either temperature extreme. During one test the converter was cooled until a significant error in reading (several counts) was detected. This occurred at approxi-

mately -50° C. No tests were run above 80° C as the epoxy potting used on some of the modules began to soften. This does not imply that 80° C is a limiting temperature for this design. With better potting materials that are currently available or different fabrication techniques, the upper limit in temperature would probably be 100° to 125° C or higher depending primarily on possible drift of the analog elements. This is substantiated by the data shown in figures 21(a) and (b), which indicate that more drift will be encountered at low temperatures than at high.

Drift with temperature for the complete converter is plotted in figure 21(a). This is the best set of data obtained and represents the ultimate accuracy attainable with this converter. Similar data were taken with somewhat different test conditions and the results of one such run are shown in figure 21(b). The reason for the deviation of these two characteristics at low temperature is not known. The data plotted in figure 21(a) were taken before the amplifier was potted but after temperature compensation had been achieved by resistor selection. All other modules were in their final form.

The amplifier was then potted and the second drift-temperature measurement made (fig. 21(b)). The deviation at low temperature was of the same form as that encountered during the process of temperature compensating the amplifier, which indicated that some unbalance had occurred. Since all of the amplifier components had been temperature cycled before use, it is unlikely that one changed value during the potting process because of the curing temperature. This leaves the possibilities of leakage due to contamination of the epoxy potting material or changes due to physical stress. In any case, potting the amplifier made further compensation impossible. It is believed that the low temperature shift experienced can be readily compensated for by the addition of a trimming potentiometer, which would also allow for final adjustment after potting. In a future design it would seem advisable tc include an external adjustment for temperature compensation.

Stability

The limited amount of testing performed on the converter to date indicates that it is quite stable having a repeatability over periods of days of one- or two-tenths of a count. The only other factor affecting its performance is noise, which proved to be a considerable nuisance in testing the converter. Because of the low level of the input, any stray noise pickup either through the power supplies or by direct radiation is a problem. The effect on the converter is to increase the width of the transition region between counts. In relation to figures 21(a) and (b) this would be evident as a broadening of the transition band. To eliminate the effects of noise during system testing extensive filtering of power supplies and shielding of the circuits was required.

Accuracy of the converter is affected not only by temperature but also by variation

in the power supply voltages. This effect is caused predominantly by the analog elements; hence, they were designed for minimum supply voltage sensitivity. Tests of the converter were run with the 6.0- and -6.0-volt supplies changed by ±5 percent of their nominal values and also with a ±10-percent variation in the 5.0-volt logic supply voltage. In each case the change in the threshold point was approximately ±0.2 count or less. This is sufficiently small for most purposes indicating that the variations used in testing can be considered practical tolerances on supply voltages. They are sufficiently broad, however, that it should not be particularly difficult to provide suitable regulated power supplies for the converter.

RECOMMENDATIONS

Considering only the performance attained with the prototype converter one would expect that with proper packaging it could be readily flight qualified. This is probably true, but there are some areas where improvement can be made to increase reliability and extend life.

Ring Counter

From the standpoint of logic design a ring counter is very desirable as it produces the desired outputs directly. In this case it produces both zero and one outputs from each stage, which fitted in well with the rest of the logic. On the debit side, the ring counter is sensitive to loading and may fall into a state where all stages are off if additional circuitry is not provided to restart it. It is also more sensitive to temperature extremes because of the biasing used to insure conduction of only one stage at a time.

There are several alternatives to the use of a ring counter. The fact that it is an eight-stage ring suggests that a three-stage binary counter could be used in conjunction with a decoding system to provide sequential outputs. Other means might be to employ a ring counter constructed from complementary flip-flops or possibly a shift register. These latter alternatives would use more components but could probably be implemented without increasing the power drain over that of the present ring counter and associated circuitry.

Use of a ring counter or shift register constructed with flip-flops would be compatible with the rest of the system as it stands since these alternates provide both an output and its complement at each stage. On the other hand, use of the three-stage counter and decoder would require modification of the flip-flop register used to drive the digital-to-analog network unless inverters were added to provide both the output and its complement. Actually, this is not necessary, and the flip-flop register can be driven directly

from parallel pulses of one polarity by a simple modification of the flip-flop triggering circuitry. This modification consists of changing the reset 2 triggering circuit so that it is enabled by a positive voltage. The enable signal can now be provided directly by the circuit replacing the ring counter, thereby eliminating the need for the gate module. Thus, it would seem possible to eliminate the present ring counter without increasing the overall parts count or power requirement of the system. The latter is particularly important if a faster conversion rate is desired. At higher operating speeds there would be a definite power saving by using complementary flip-flops rather than the more conventionally designed ring counter.

Noise

Another problem encountered in this converter that would not be as severe in an all digital system was that of noise. Complementary digital circuits have nearly ideal performance but also present a noise problem. When these circuits change state, both transistors are turned on for a very short time - approximately the circuit rise time. This is caused by minority carrier storage in the transistor being turned off. The result is that the circuit draws a high current during this time, which is typically 50 to 100 nanoseconds. The fast spikes appearing on the supply line propagate throughout the system and may cause false triggering. Naturally, systems including amplifiers such as the analog-to-digital converter will be particularly noise sensitive. Not only will they be sensitive to switching noise generated within the system but also to noise from the power supplies or pickup by radiation. A more satisfactory cure than the extensive shielding and filtering used when testing the prototype converter would be to eliminate noise at its point of entry into the system. This would require decoupling networks in each module as well as careful system packaging.

DISCUSSION

Performance of the prototype analog-to-digital converter indicates that an absolute accuracy of ± 1 count is attainable with a total power drain of less than 10 milliwatts. With a full scale input of 20 millivolts and conversion to seven bits, one count corresponds to 160 microvolts, which should be sufficient sensitivity for nearly all space vehicle applications. A flight-qualified converter built to this general design should, therefore, be applicable to a large percentage of future space shots. Although not specifically built for flight, the design and construction of the converter embodied most of the requirements of a flight system, and only minor modifications would be required to produce a fully flight-qualifiable unit.

Apart from their use in the converter, all of the circuits developed are suitable for applications where power is severely limited. They should prove advantageous for all types of satellite and space probe systems ranging in complexity from a simple signal conditioner for a single experiment to construction of a complete on-board data processing system. This analog-to-digital converter is well suited as an input conversion device for such a data system.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, March 26, 1965.

APPENDIX - READOUT CARD

The readout card was designed and built to facilitate testing and demonstration of the analog-to-digital converter. As part of a larger data system, the contents of the analog-to-digital converter storage register would be processed and transmitted in binary form; however, during testing, a binary-to-decimal converter was desirable for quick and accurate monitoring of the analog-to-digital storage register contents. Also, since the analog-to-digital converter took 250 words per second, a buffering or sampling operation was necessary between the analog-to-digital converter, and the decimal display device to provide a lower readout rate.

The readout card samples, in parallel, the output of the analog-to-digital storage register at approximately 1-second intervals (the minimum display time of the digital counter used) and converts this to a serial pulse train of from 0 to 127 pulses (1 pulse for each count). The serial pulses are then counted by a commercial laboratory digital counter. A gate pulse is also provided to the digital counter in order to define the beginning and end of the pulse train.

The logic diagram of the readout card is shown in figure 22. The eight flip-flops are interconnected as an eight-stage counter with parallel entry into seven lower order stages and the eighth stage used to detect overflow. Two monostable multivibrators (one shots) of approximately equal time constants are used to set the sample rate. The second one shot serves to lock out the first so as to allow it sufficient recovery time between cycles.

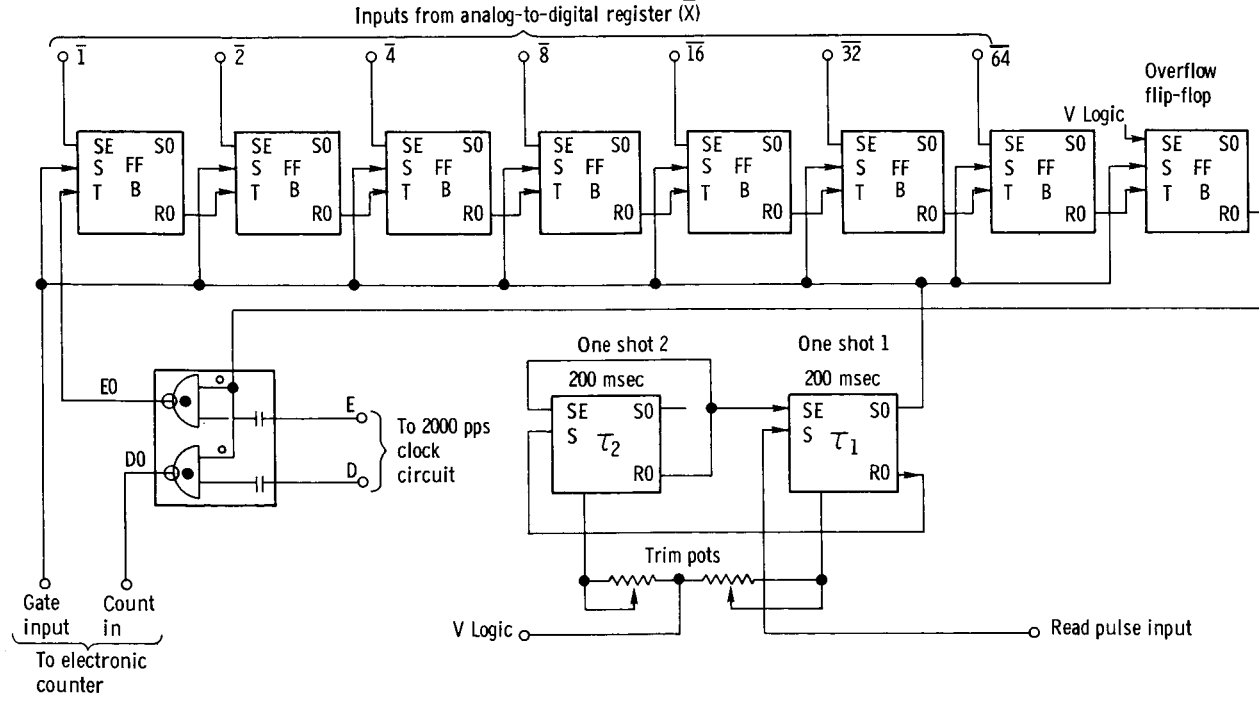


Figure 22. - Readout card.

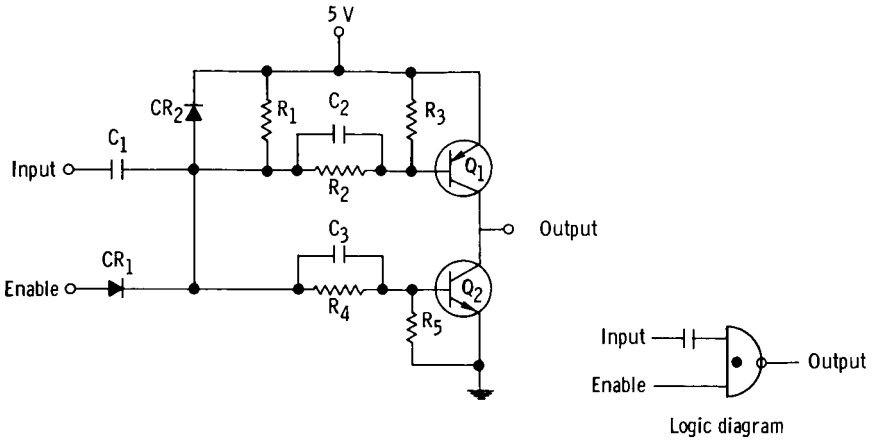


Figure 23. - Complementary transistor NAND gate.

When the read pulse (p. 7) occurs and both one shots are in the stable states, one shot number 1 is set. One shot number 1, in turn, gates the complement of the contents of the analog-to-digital converter storage register ($\overline{X}$) into the seven lower-order flip-flop stages of the readout system, sets the overflow flip-flop, and provides a reset pulse to the digital counter. Setting the overflow flip-flop removes the inhibit from both complementary NAND gates, and staggered clock pulses are sent to the digital counter and to the eight-stage binary counter. When overflow occurs, the overflow flip-flop is reset, which in turn inhibits the NAND gates and stops the count. The total number of pulses delivered to the eight-stage binary counter is

$$m = 128 - \overline{X}$$

but, as stated on page 23,

$$\overline{X} = 127 - X$$

Therefore,

$$m = X + 1$$

When a staggered clock and two NAND gates are used, the extra pulse is eliminated so that the number of pulses delivered to the external digital counter is X (the contents of the analog-to-digital storage register). Note that at the end of the count cycle all readout card flip-flops are in the reset state, which eliminates the need for special register reset circuitry.

The flip-flops used are similar to figure 4 (p. 10) except that a standard toggle input was provided and the two reset circuits were eliminated. Also, the end of R_{13} returned

to 5 volts is instead brought out as a set enable.

The one shots are similar to that shown in figure 6 (p. 11) except C_4 was changed to 1 microfarad and R_6 to 270 kilohms, and set enables were added exactly as before.

Active load complementary NAND gates (see fig. 23) were used in lieu of the passive load stacked transistor type used in the analog-to-digital converter in order to provide a low impedance output to drive the external digital counter.

The completed readout card is shown with the converter in figure 18 (p. 22). Since the card was not a part of the analog-to-digital converter, it was operated from a separate 5-volt supply and did not undergo temperature testing with the converter. However, because complementary circuits were used exclusively throughout, power consumption was necessarily low.

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